
black hat
MIDDLE EAST AND AFRICA
(M)Wait for it
Bridging the Gap between Microarchitectural and Architectural Side Channels
15 - 17 NOVEMBER 2022
RIYADH FRONT EXHIBITION CENTRE
SAUDI ARABIA
Ruiyi Zhang, Daniel Weber, Michael Schwarz
CO-ORGANISED BY:
informatech
IN PARTNERSHIP WITH:
Riyadh

# Who am I?

**Ruiyi Zhang**

PhD Student @ CISPA Helmholtz Center for Information Security

@Rayiizzz

ruiyi.zhang@cispa.de

# Who am I?

**Daniel Weber**

PhD Student @ CISPA Helmholtz Center for Information Security

@weber_daniel

daniel.weber@cispa.de

# Who am I?

**Michael Schwarz**

Faculty @ CISPA Helmholtz Center for Information Security

@misc0110

michael.schwarz@cispa.de

# About this presentation

This talk is about how the power-optimization instructions *UMONITOR/UMWAIT* leak information

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This talk is about how the power-optimization instructions *UMONITOR/UMWAIT* leak information

- Not about software bugs
- A side channel to leak information
- Not due to the hardware design, but due to the instructions themselves

# Livedemo: Spectral

# What can we do

- Combined with transient-execution attacks

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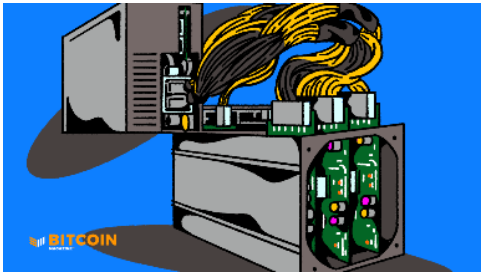
- Combined with transient-execution attacks
- Cross-vm Cross-CPU covert channel
- Leakage of cryptographic keys
- Mainly focus on the Intel's newest CPUs (since Alder Lake and Tremont-based)
- But a generic interrupt-timing attack is also available on AMD and ARM


ENERGY CRISIS

# Heat Your Home with Bitcoin Mining




Build an additional heating system from mining cryptocurrency

- Repurposing the waste heat

Warren, R. (2022, March 25). *HOW TO HEAT YOUR HOME WITH BITCOIN MINING*. Bitcoin Magazine. https://bitcoinmagazine.com/business/how-to-heat-your-home-with-bitcoin-mining

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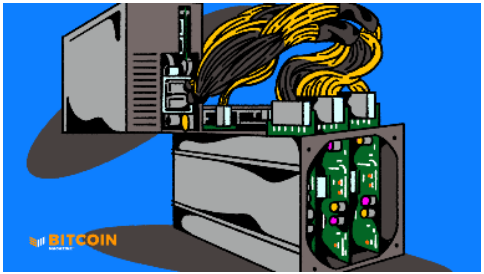


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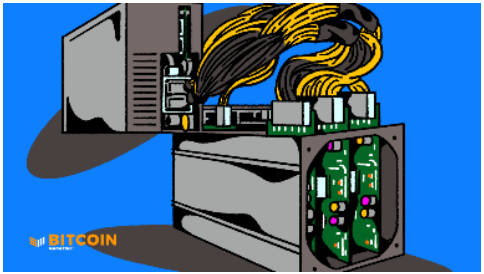


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 (for longer lifespan of CPU)

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# How does a Processor Save Energy?

CAN'T WASTE POWER


IF YOU DON'T TURN ON IT

# How does a Processor Save Energy?

Idle

Busy

# How does a Processor Save Energy?

Idle

Busy

- Idle the processor

# How does a Processor Save Energy?

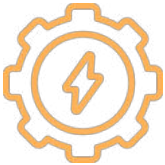
Idle

- Idle the processor

Busy

- Lower the voltage
- Decrease the frequency

# Processor Power Management



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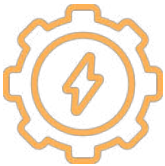
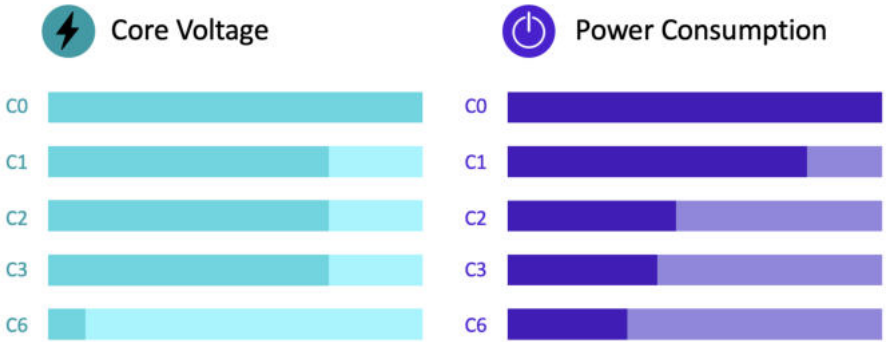
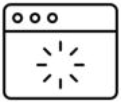


- Modern processors support multiple technologies to optimize the power consumption:
  - CPUIdle driver
  - Scaling drivers (intel_pstate, intel_cpufreq, ...)
- Which corresponds to ...
  - C-states (Idle States)
  - P-states (Performance States)

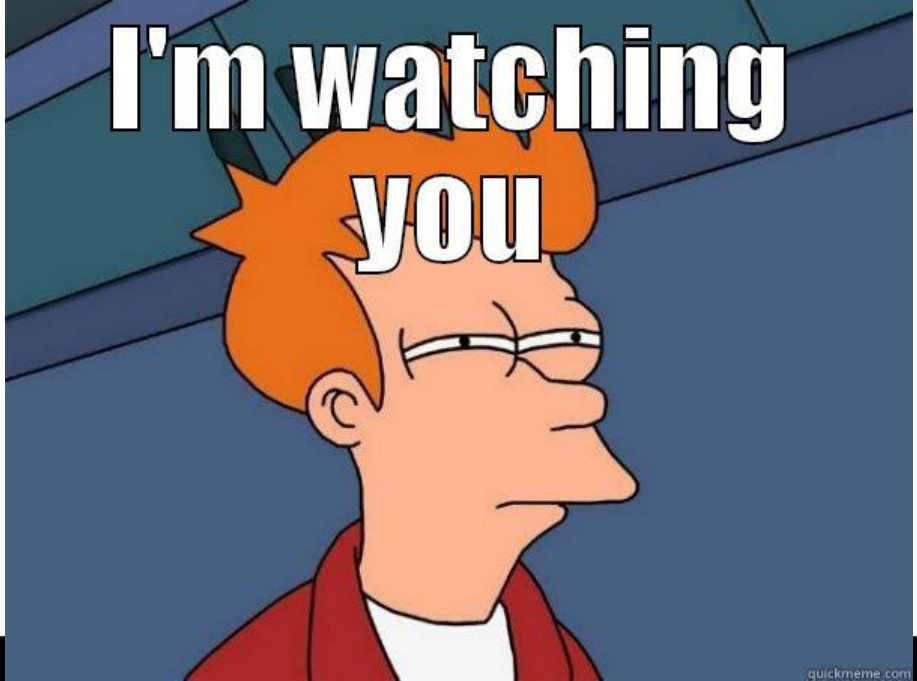
# Idle States





## Privileged Instructions

- (↓C1) HLT - Halt
  - Stops instruction execution, puts the processor in a HALT state
  - Wakes up by interrupts
  - Can be configured to restart after interrupts
- (↓Cx) MONITOR/MWAIT


I'm watching you
quickmeme.com

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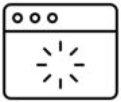
  - The bit 1 of ECX of MWAIT indicates this feature is used
  - The maximum waiting time is an implicit 64-bit timestamp-counter value stored in the EDX:EBX register pair



## Unprivileged Instructions

- (↓C0.2) TPAUSE - Timed PAUSE (Intel)
- (↓C0.2) UMONITOR/UMWAIT (Intel)
- (↓C1) MONITORX/MWAITX (AMD)

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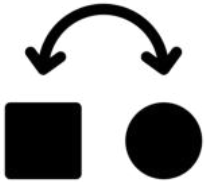
- A store to the monitored memory range
- Interrupts
- User-defined timeout (the implicit EDX:EAX 64-bit input value)
- OS-defined timeout (writing TSC-quanta value to MSR 0xe1)

# Architectural Difference



If the processor exits the optimized state due to the OS-defined timeout, the UMWAIT instruction sets RFLAGS.CF

# MONITOR / MWAIT

- MONITOR: Set up an address range for the monitor hardware
- MWAIT: Wait until a write-back store is performed within the range specified by the instruction MONITOR
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# How does UMONITOR/UMWAIT Spy on a Memory Range?

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Monitored Address

# How does UMONITOR/UMWAIT Spy on a Memory Range?


Monitored Address


Aliased Address

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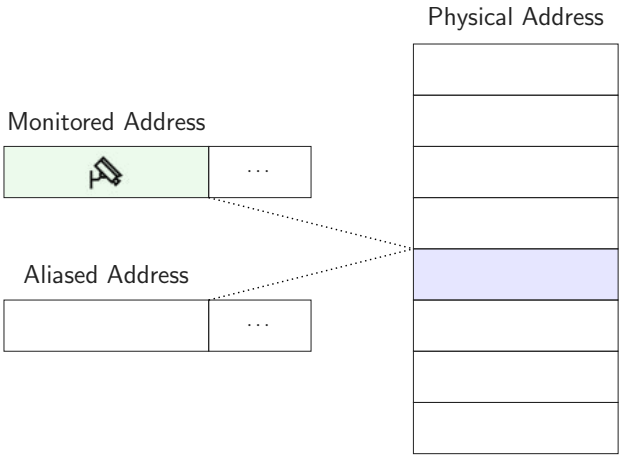

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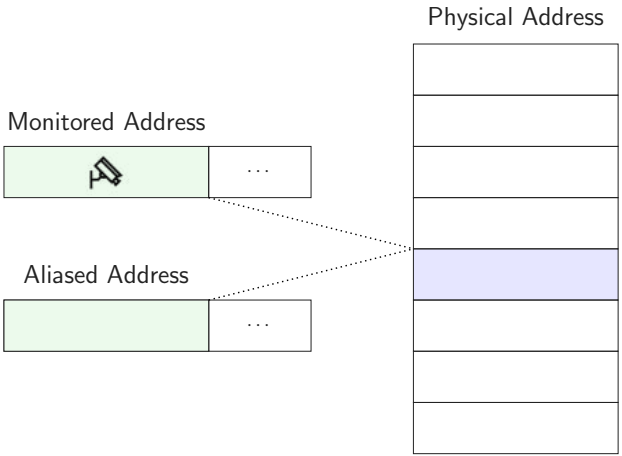

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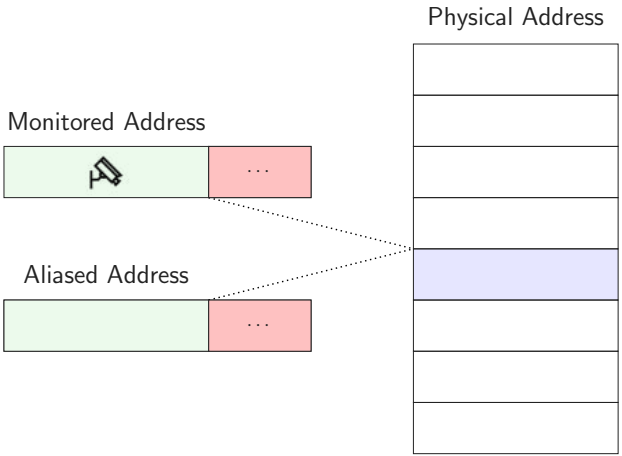
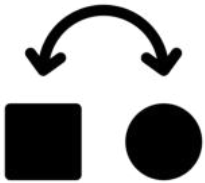


# How does UMONITOR/UMWAIT Spy on a Memory Range?

| Access | Trigger | UMONITOR | MONITORX | MONITOR |
|---|---|---|---|---|
| *architectural* | Write | ✓ | ✓ | ✓ |
| | Flush | ✗ | ✓ | ✓ |
| | `clzero` | N/A | ✓ | ✓ |
| | `clwb` | N/A | † | † |
| | `prefetchw` | ✓ | † | † |
| *transient* | Speculative write | ✓ | † | † |
| | Write after exception | ✓ | † | † |

† only on Zen 3, not on Zen or Zen+

# Architectural Feedback for Microarchitectural State

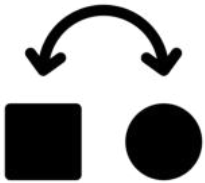


- Modification to the monitored microarchitectural state → RFLAGS.CF=0
- Interrupts → RFLAGS.CF=0
- User-defined timeout → RFLAGS.CF=0

---

- OS-defined timeout → RFLAGS.CF=1

# Architectural Feedback for Microarchitectural State



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→ A side channel to convert the microarchitectural state into architectural state

# Attack Primitive #1: Transient-Write Monitor

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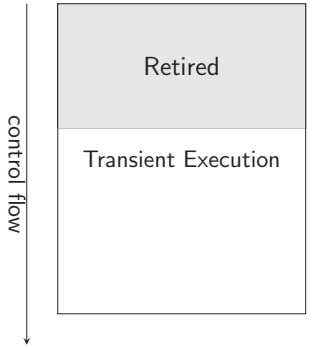
Victim - Core #$X$



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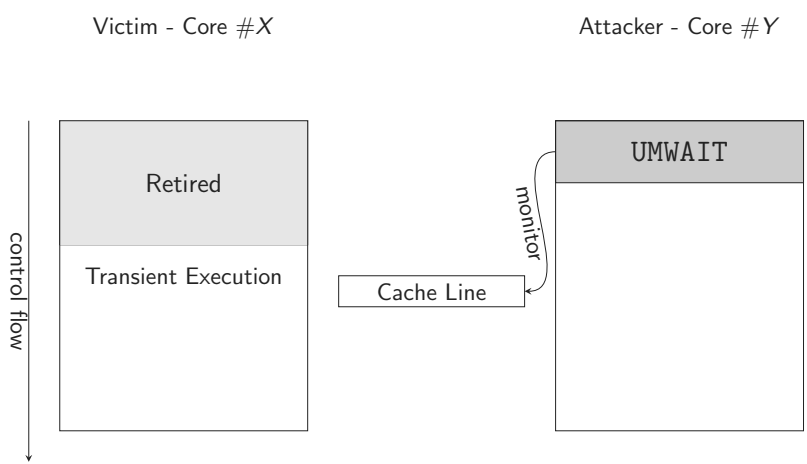

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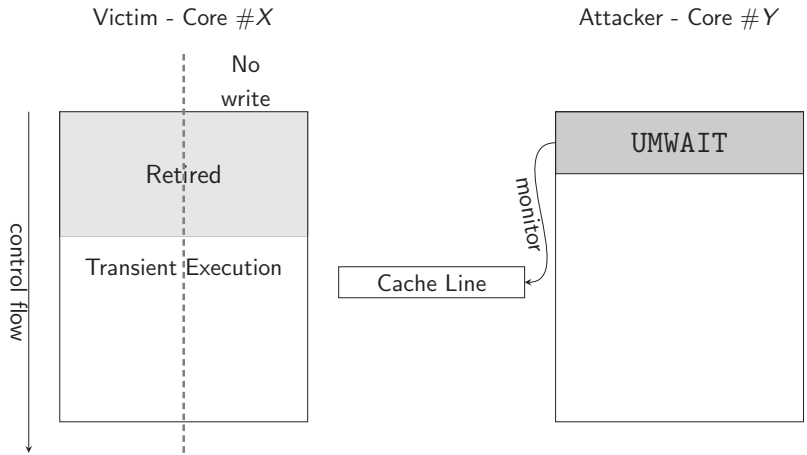

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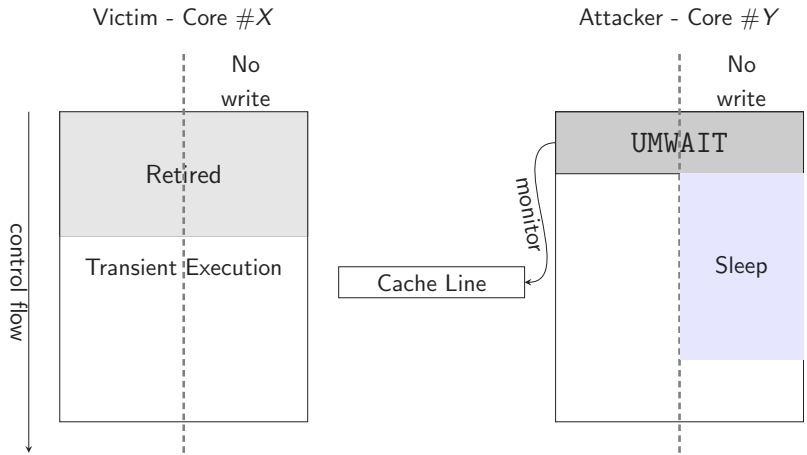

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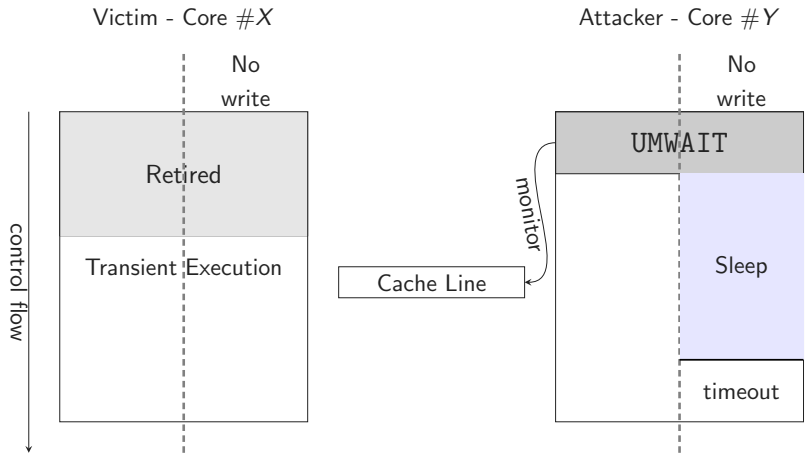

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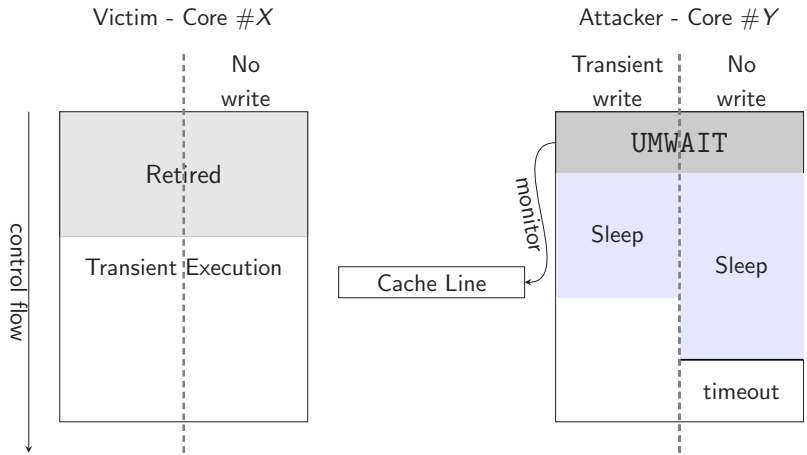

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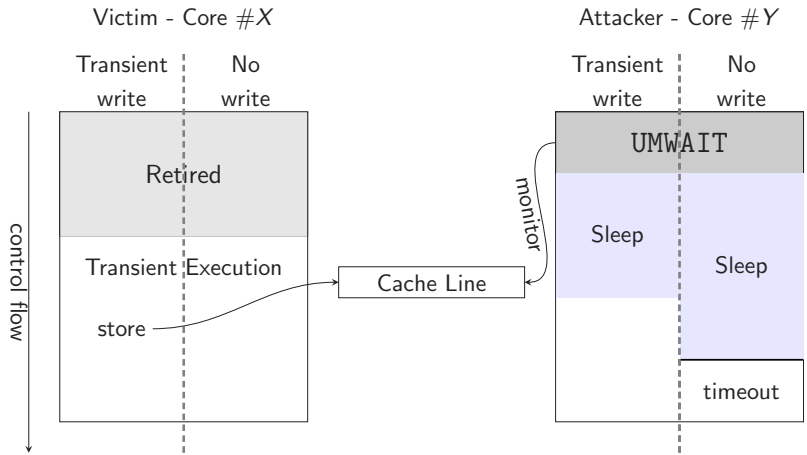

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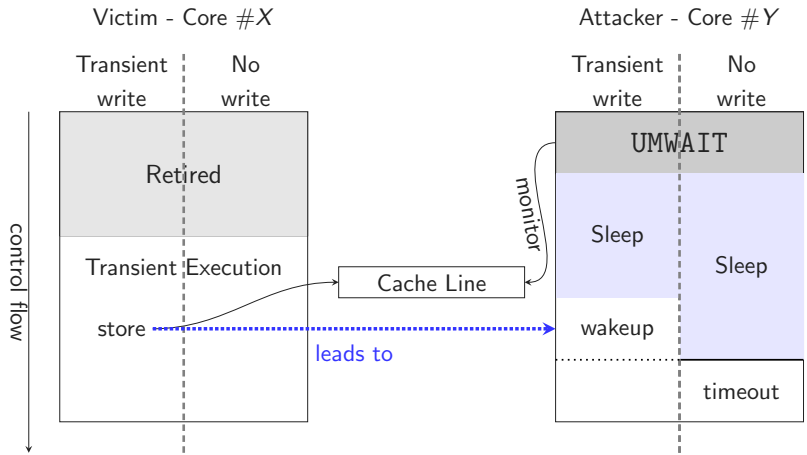

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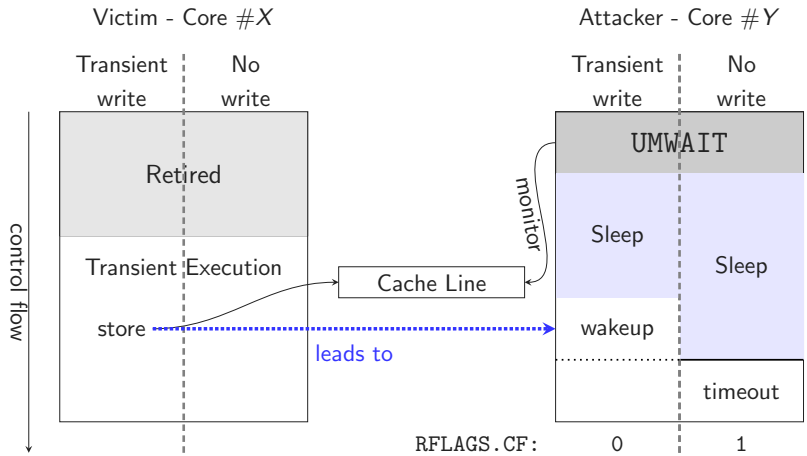


# Properties

Low noise

# Properties

Low noise

High accuracy

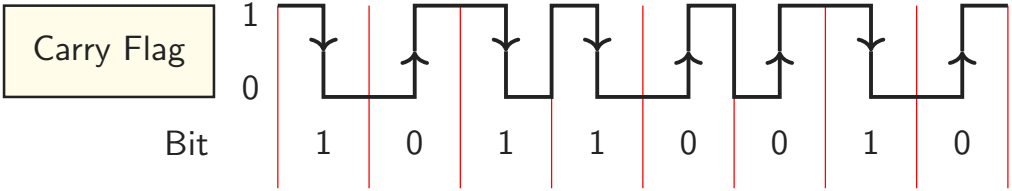
# Properties

Low noise

High accuracy

Stealthy

# UMWAIT Covert Channel



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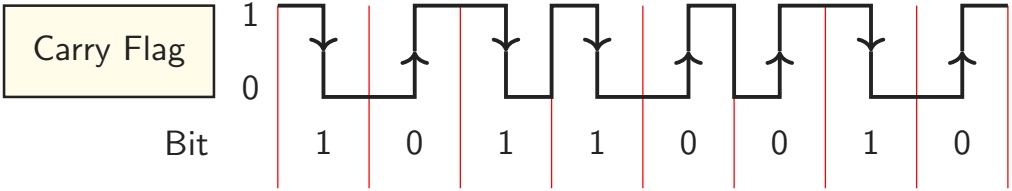


- Cross-core cross-VM covert channel
- 697 bit/s
- 0% error rate

# Spectre with Architectural Leakage

```
if ( x < array1_size)
  array2[(array1[x] * 64)] = ...;
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Monitor the cache line | array2[0]

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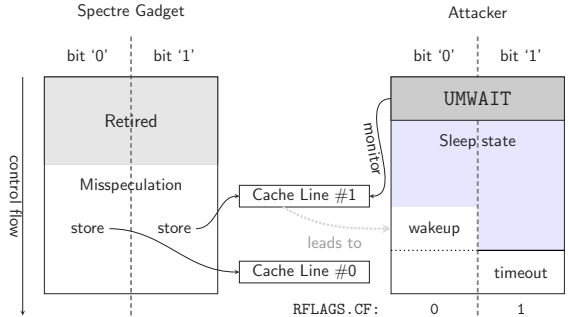

# Attack Primitive #2: Timer-less Timing Measurement

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- Distinguish fast events from slow events

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- Distinguish fast events from slow events
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  → Timestamp Counter

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  - → ... ...

# Attack Primitive #2: Timer-Less Timing Measurement

```
memory access
```

# Attack Primitive #2: Timer-Less Timing Measurement

```
start = ⏱
 memory access
end = ⏱
```

# Attack Primitive #2: Timer-Less Timing Measurement

```
start = ⏱
 memory access
end = ⏱
Δ = end - start
```

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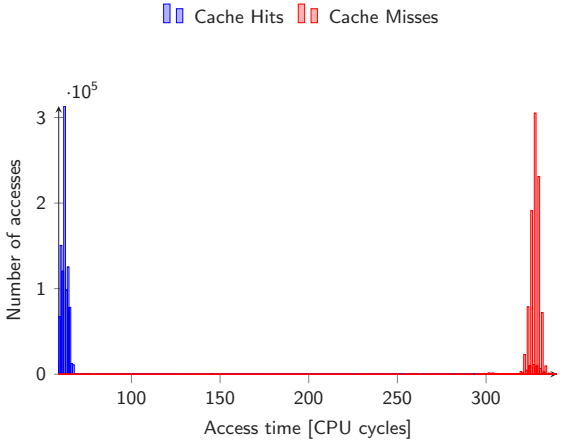

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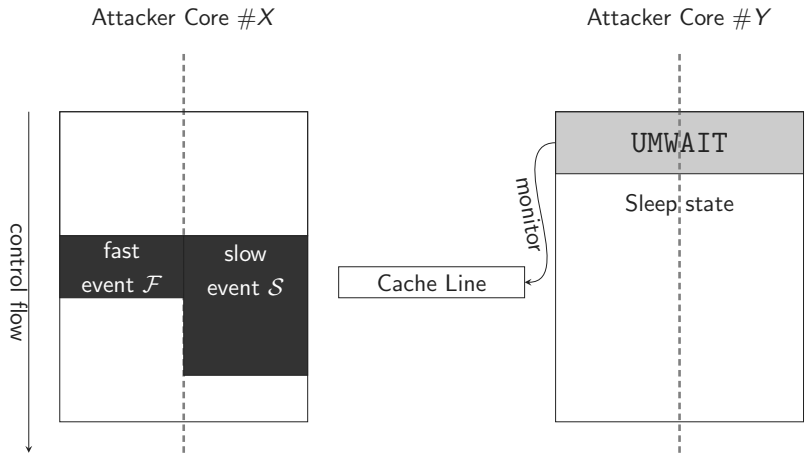

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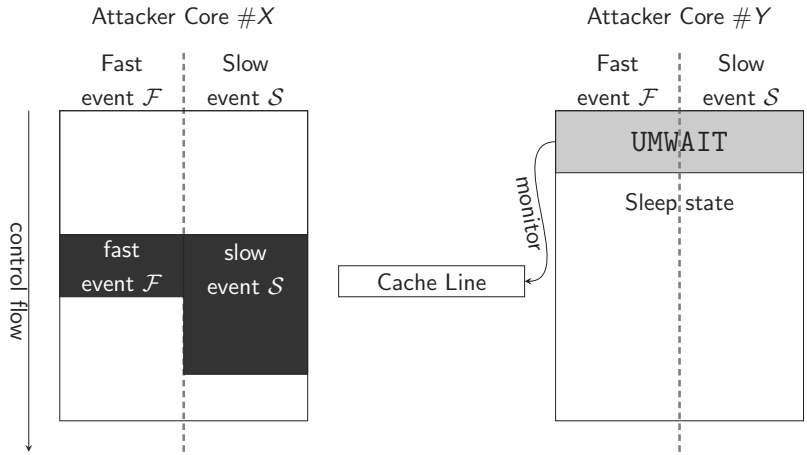

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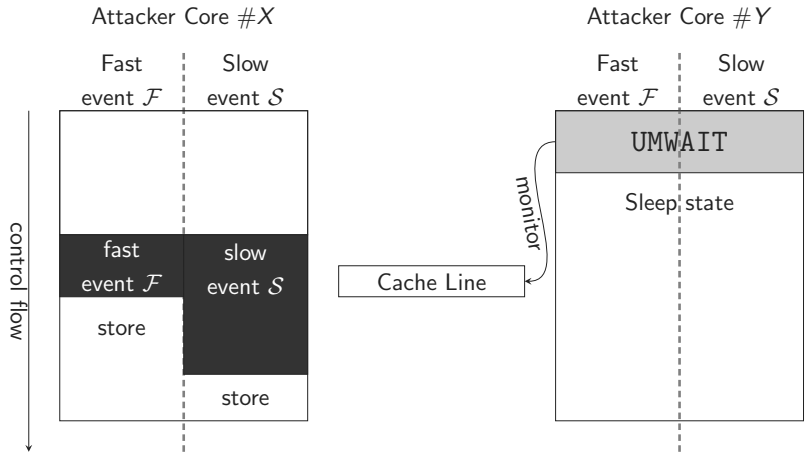

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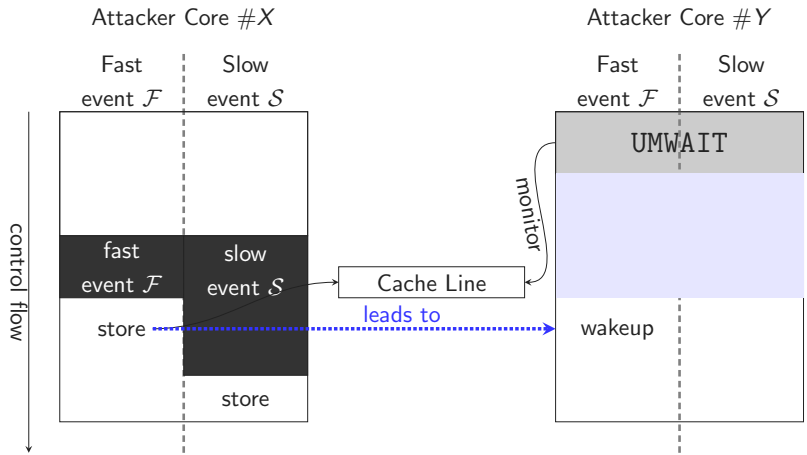

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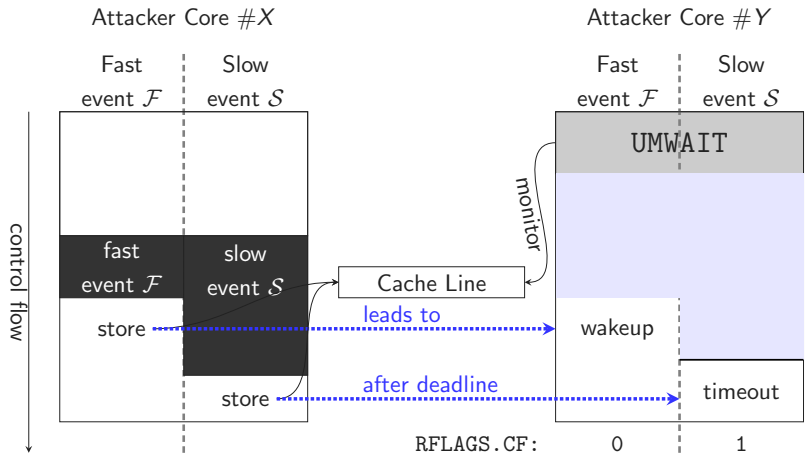

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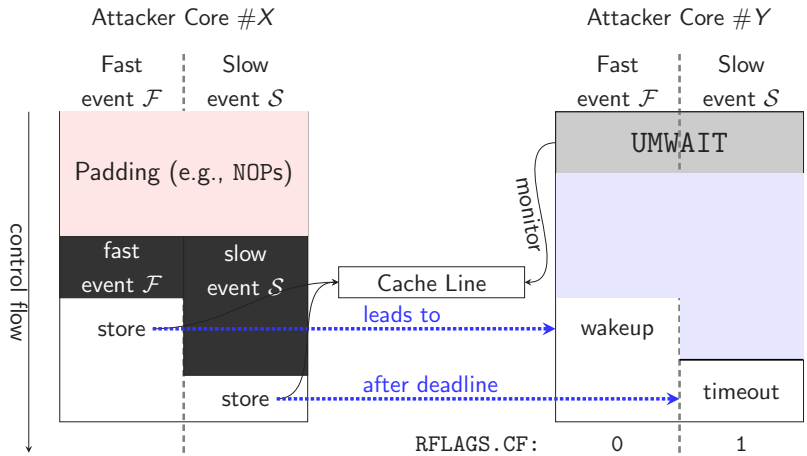
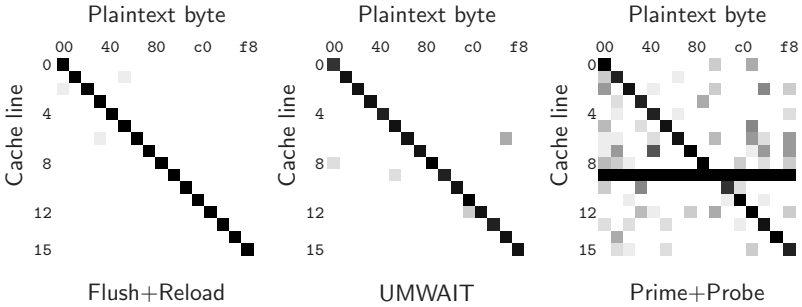


# AES Key Leakage



# Attack Primitive #3: Monitoring Interrupts

# Measuring Time

```
start = ⏱
end = ⏱
```

# Measuring Time

```
start = ⏱
end = ⏱
Δ = end - start
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1. run: $\Delta = 12$

# Measuring Time

```
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end = ⏱
Δ = end - start
```

1. run: Δ = 12
2. run: Δ = 12

# Measuring Time

```
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end = ⏱
Δ = end - start
```
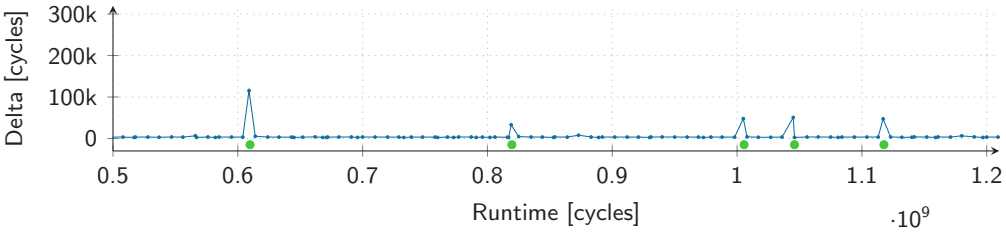

1. run: Δ = 12
2. run: Δ = 12



# Interrupt-timing Attacks

```
int now = rdtsc();
while (true) {
  int last = now;
  now = rdtsc();
  if ((now - last) > threshold) {
    reportEvent(now, now - last);
  }
}
```

- Schwarz, M., Lipp, M., Gruss, D., Weiser, S., Maurice, C., Spreitzer, R., & Mangard, S "Keydrown: Eliminating software-based keystroke timing side-channel attacks.; NDSS 2018

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- Continuously acquire high-resolution timestamp

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- Continuously acquire high-resolution timestamp
- Interrupt → large difference between timestamps

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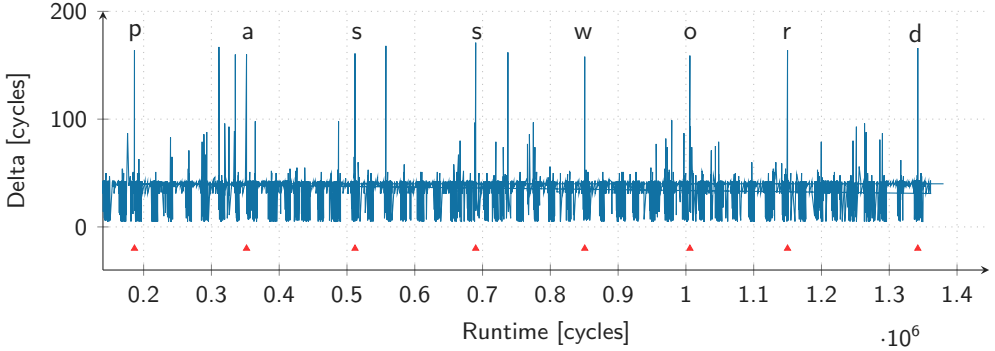


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# Attack Primitive #3: Monitoring Interrupts

- Intel: UMONITOR/UMWAIT & TPAUSE
- AMD: MONITORX/MWAITX
- ARM: WFI

# Attack Primitive #3: Monitoring Interrupts

E.g., the timeout of MWAITX is a 32-bit value → 2s for a 2 GHz CPU

App

OS

Δ

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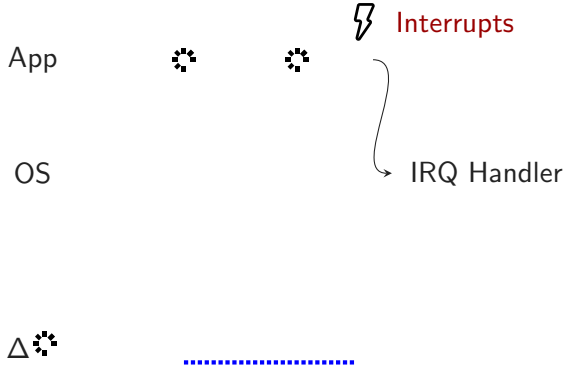

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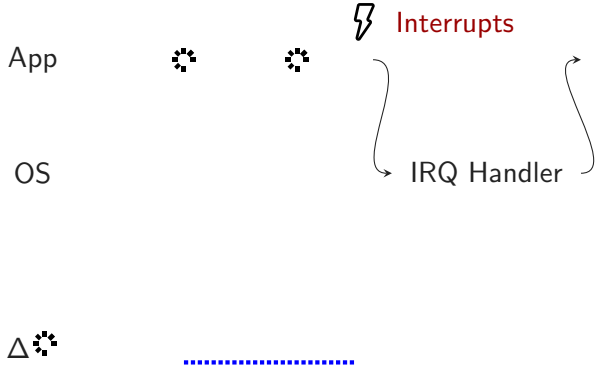

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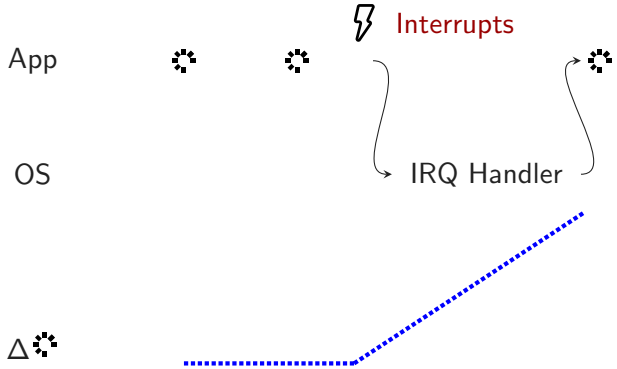

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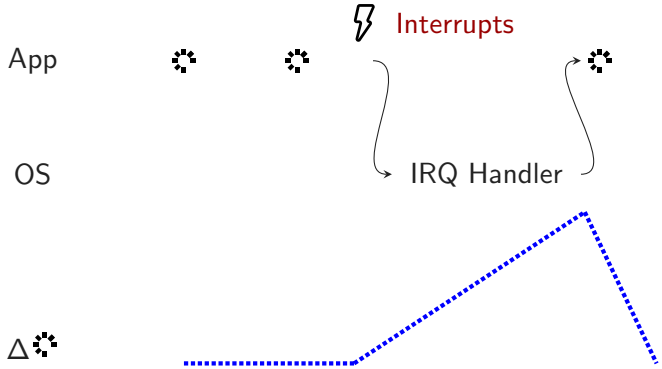

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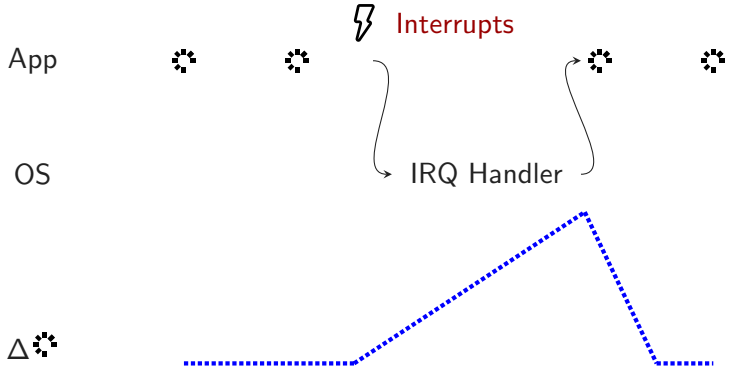
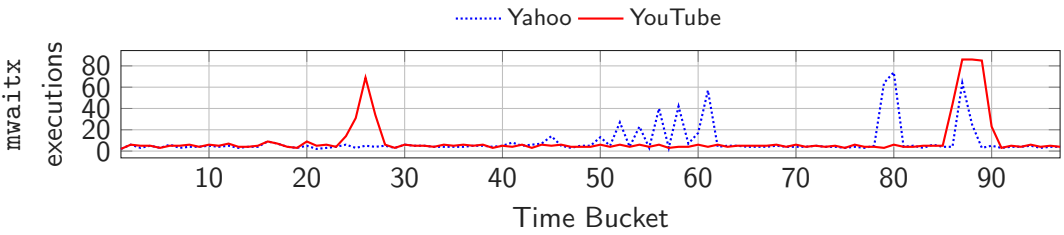
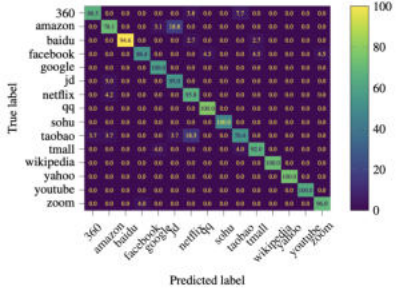


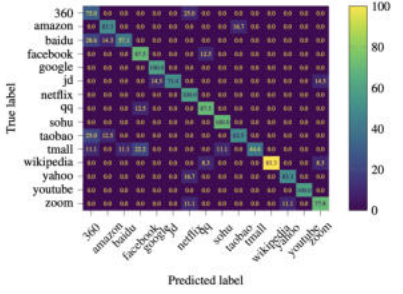
# Monitoring Network Interrupts



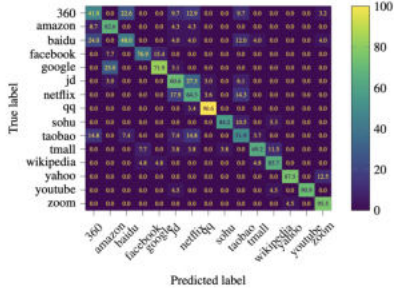
# Website Fingerprinting Attack




(a) AMD



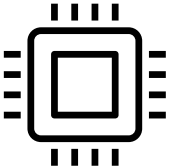

(b) ARM



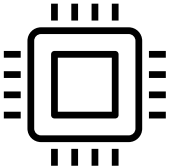

(c) Intel

# Countermeasures

# Countermeasures - Hardware



# Countermeasures - Hardware



- Remove wake-up reason

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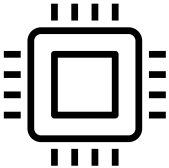
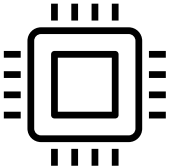


- Remove wake-up reason
- Remove functionality

# Countermeasures - Hardware



- Remove wake-up reason
- Remove functionality
- Instruction deprecation

# Countermeasures - Operating System

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- Remove the umwait OS timeout

# Countermeasures - Software

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- Spectre mitigations

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- Spectre mitigations
- Constant-time implementations
- (Introduce artificial noise)

# Take Aways

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→ `https://github.com/cispa/mwait`


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